IN THE DRAWINGS:

In Figure 13 of the drawings, the lead line and the numeral 21A has been added. Also in Figure 18 of the drawings one occurrence of T1 has been changed to T2, the lead line and the numeral 72 has been added, and the direction of one of the arrows associated with the CPG 71 has been changed. Submitted concurrently herewith is a Letter to the Office Draftsperson submitting replacement drawing sheets for Figures 13 and 18 including the above identified corrections. Entry of these drawing corrections is respectfully requested.

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated July 25, 2005 (Paper No. 1). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Also, submitted concurrently herewith is an Information Disclosure Statement. Entry and consideration of this Information Disclosure Statement is respectfully requested.

Status of the Claims

Claims 1 through 15, 23 and 24 are currently pending in the above-identified application. Claims 16 through 22 have been previously cancelled without prejudice or disclaimer. Also, Claims 1, 5, 8 through 14, 23 and 24 are being amended to correct formal errors, place the claims in better form and to more particularly point out and distinctly claim the subject invention. Entry of the amendments to Claims 1, 5, 8 through 14, 23 and 24 is respectfully requested.

Additional Amendments

The Specification and the Abstract of the Disclosure have been amended to correct formal errors and to better disclose and describe the features of the present invention. Entry of the amendments to the Specification and to the Abstract of the Disclosure is respectfully requested.

In Figure 13 of the drawings, the lead line and the numeral 21A has been added. Also in Figure 18 of the drawings one occurrence of T1 has been changed to T2, the lead line and the numeral 72 has been added, and the direction of one of the arrows associated with the CPG 71 has been changed. Entry of these drawing corrections is respectfully requested.

Formal Objections/Rejections

The Abstract of the Disclosure was objected to in view of its length. In response, attached to this response is a Substitute Abstract of the Disclosure which addresses this objection to the Abstract of the Disclosure. Therefore, withdrawal of the objection to the Abstract of the Disclosure is respectfully requested.

Prior Art Rejections

Claims 1 through 15, 23 and 24 were rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,535,415 to Takemura et al., hereinafter the Takemura '415 patent. This rejection is respectfully traversed.

Semiconductor integrated circuits of the present invention, such as respectively recited in Claims 1 through 15, 23 and 24, include a central processing unit, a memory, and clock generator.

The semiconductor integrated circuits of the present invention have a plurality of operation states or modes including an active state, or active mode, and a standby state, or standby mode. The semiconductor integrated circuits of the present invention change the active state, or active mode, to the standby state or standby mode, when the central processing unit executes a predetermined instruction.

In the active state, the central processing unit can access the memory and is provided a clock signal from the clock generator. Also, the memory typically can desirably have voltage generation circuits for bit lines and source lines with which memory cells are connected. In response to an instruction to transition from the standby state, or standby mode, to the active state or active mode, the voltage generation circuits produce a potential difference between the bit lines and the source lines.

In the standby state, or standby mode, the central processing unit stops operation and the clock generator stops generating the clock signals. In response to an instruction to transition from active state, or active mode, to standby state, or standby mode, the voltage generation circuits desirably make the potential of the bit lines and that of the source lines equal to each other.

Therefore, in the semiconductor circuits of the present invention, the central processing unit controls changes of the operation states, or operation modes, and the central processing unit is enabled or disabled to access the memory according to the operation state. Also, the potential, the charging or the discharging of the bit lines and the source lines of the memory are controlled according to the operation state or operation mode.

The Takemura '415 patent discloses that a semiconductor device includes memory cells, data lines (D1t, D1b, etc), word lines (WL), and common source lines (CSP, CSN) (See Figure 1 the Takemura '415 patent), and that a power source of the data lines and a power source of the common source lines are controlled in an active and a standby state (See Figures 20 and 21 of the Takemura '415 patent).

However, in contrast, it is respectfully submitted that the Takemura '415 patent does not disclose a semiconductor device that has a central processing unit which is able to access the memory in a predetermined state or mode, such as the active state or active mode. Further, the Takemura '415 patent does not disclose that an operation state or mode, such as the active state, or active mode or the standby state, or standby mode, is controlled by the central processing unit, such as by the central processing unit executing a predetermined instruction. Also, the Takemura '415 patent does not disclose that the memory is not accessed by the central processing unit in a predetermined state or mode, such as the standby state or mode, in which the central processing unit is not provided a clock signal.

Therefore, in view of the foregoing, it is respectfully submitted that the Takemura '415 patent does not anticipate the semiconductor integrated circuits as respectively recited in Claims 1 through 15, 23 and 24.

Withdrawal of the 35 U.S.C. § 102(e) rejection of Claims 1 through 15, 23 and 24 is respectfully requested.

Reconsideration and allowance of Claims 1 through 15, 23 and 24 are respectfully requested.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejection in the Office Action relies. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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